CLAIMS:

What is claimed is:

1. A data processing system comprising:

an interconnect;

a processor that processes memory access requests in program order;

a memory system coupled to said processor which supports memory access requests in a weakly consistent order; and

a controller that issues said memory access requests to said memory system and places a barrier operation on said interconnect in response to each memory access request issued.

2. The data processing system of Claim 1, wherein said controller includes means for creating said barrier operations.

3. The data processing system of Claim 1, wherein said controller includes means for speculatively issuing load requests to said memory system while a barrier operation is pending.

4. The data processing system of claim 3, wherein said controller includes means for allowing data returned by a speculatively issued load request to be utilized by said processor only when an acknowledgment is received from all barrier operations pending when said load was issued.

5. A processor comprising:

an instruction sequencing unit (ISU) that receives memory access instructions in program order;

a load store unit (LSU) including a controller that issues memory access requests associated with said memory access instructions to an interconnect and places a barrier operation on said interconnect in response to each memory access request issued.

6. The processor of Claim 5, wherein said controller includes means for creating said barrier operations.

7. The data processing system of Claim 5, wherein said controller includes means for speculatively issuing load requests to said interconnect while a barrier operation is pending.

8. The data processing system of claim 7, wherein said controller includes means for allowing data returned by a speculatively issued load request to be utilized by said processor only when an acknowledgment is received from all barrier operations pending when said load was issued.

9. A method of processing instructions in a data processing system, said method comprising the steps of:

receiving an instruction sequence at a processor in program order, said instruction sequence including a memory access instruction;

in response to receipt of said memory access instruction, creating a memory access request and a barrier operation;

placing said barrier operation on an interconnect after said memory access request is issued to a memory system; and

upon completion of said barrier operation, completing said memory access request in program order.

10. The method of Claim 9, wherein said memory access request is a load request and further including the step of speculatively issuing said load request while a barrier operation is pending.

11. The method of Claim 10, further including the step of forwarding data returned by said speculatively issued load request to a register or execution unit of said processor, when an acknowledgment is received for said barrier operation.